SIDDHARTH INSTITUTE OF ENGINEERING AND TECHNOLOGY :: PUTTUR (AUTONOMOUS)

Siddharth Nagar, Narayanavanam Road - 517583

QUESTION BANK

Subject with Code : <u>Advanced DSP& Applications</u>(16EC5504)

Course & Branch: M.Tech – (ES)

Year & Sem: I-M.Tech & I-Sem

<u>UNIT-I</u>

LIT DISCRETE-TIMESYSTEMS IN THE TRANSFORM DOMAIN

1.(a) Discuss the principle of extracting minimum phase function from the magnitude	
spectrum for digital filters.	[5M]
(b)Determine the minimum phase transfer function following magnitude squared function	[5M]
for the given $H(j\Omega) = \frac{5+4\cos(\Omega)}{17+8\cos(\Omega)}$	
2.(a) Explain about the poly phase filters structures and how they are used in interpolation.	[5M]
(b) Write down differences between FIR and IIR filter	[5M]
3. (a) Design of linear phase FIR filters using windows.	[5M]
(b)Write the different types of linear – phase transfer functions	[5M]
4. (a) Explain about IIR trapped cascaded lattice filters.	[5M]
(b).Write a short note digital sine-cosine generator.	[5M]
5. (a) Consider two LTI causal digital filters with impulse responses given by:	[5M]
$\begin{split} h_1(n) &= 0.5\delta(n) - \delta(n-1) + 0.5\delta(n-2) \\ h_2(n) &= 0.5\delta(n) + \delta(n-1) + 0.5\delta(n-2) \end{split}$	
Sketch the magnitude response of the two filters and compare their characteristics	
(b) State and explain the process of deconvolution in inverse systems with suitable example	[5M]
6. (a) Draw the cascaded lattice structure that can be used to realize an arbitrary FIR	
transfer function and develop the realization algorithm for the same.	[5M]
(b) Derive a single multiplier structure for generating sine-cosine sequences from a	
general second order digital filter structure.	[5M]
7. (a) Explain algebraic stability test	[5M]
(b) With an example explain the all pass realization of IIR transfer functions	[5M]
8. (a) Physically realizable and stable IIR filters cannot have linear phase. Prove	[5M]
(b) Describe the characteristics of IIR and FIR systems.	[5M]

	QUESTION BANK	2016
9.(a) Explain the poly-phase digital filter structure		[5M]
(b)Explain state space structure and poly phase structure.		[5M]
10.(a) What is an all pass filter and write down in properties?		[5M]
(b). (i) Define a casual system.		[5M]
(ii)Differentiate stable from a unstable system.		

Prepared by: **B.VENKATESU**



SIDDHARTH GROUP OF INSTITUTIONS :: PUTTUR

Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK (DESCRIPTIVE)

Subject with Code : ADSP&A(16EC5504)

Branch& Specialization: ECE-ES

Year & Sem: M.TECH-I SEM

<u>UNIT-II</u>

1.(a) Explain the design of an IIR filter using Pades's approximation method.	[5M]
(b)Explain the advantages of Pades's approximation method.	[5M]
2. (a).Explain the method of designing IIR filters using Pade approximation	[5M]
(b) Explain the complexity of digital filter structure	[5M]
3. (a) What are the advantages of FIR filter?	[5M]
(b). Write a short note on narrow frequency band of DFT.	[5M]
4.(a). Discuss about fast DFT algorithm based on index mapping	[5M]
(b). Explain about least square design method	[5M]
5.(a) Compare the filter design for FIR and IIR filter.	[5M]
(b). If $H(S) = 2$	
(S+1)(S+4)	[5M]
determine $H(Z)$ using impulse invariance method for T = 0.1 sec & 1 sec	
6. What do you understand by pade approximation method to design an IIR filter?	[10M]
In what respect, this method is different from the method of frequency transformation	
7. Explain the design of computationally Efficient FIR Filters.	[10M]
8. (a) Explain the principle of spectral transformations of IIR filters.	[5M]
(b). What are the issues in the design of FIR filters?	[5M]
9. List out the least square design methods ?Explain each with one example.	[10M]
10. A band limited analog signal is sampled (with no aliasing) at 500 Hz and	[10M]
980 samples are collected. DFT of these 980 samples is computed. It is desired to	
compute The value of the spectrum of the esampled signal at 120 Hz.	
(i)Which DFT index is nearest to 120 Hz and what is its physical frequency in hertz?	
(ii)What is the minimum number of zeros that need to be padded onto the 980 samples	
to obtain a DFT at 120 Hz exactly? What is the DFT index k then corresponding to 120 H	Ηz.
Prepared by: B.VENKA	ATESU

SIDDHARTH GROUP OF INSTITUTIONS :: PUTTUR

Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK (DESCRIPTIVE)

Subject with Code : ADSP&A(16EC5504)

Branch& Specialization: ECE-ES

Year & Sem: M.TECH-I SEM

<u>UNIT –III</u>

DSP ALGORITHMS

[5M]
[5M]
[5M]
[5M]
[5M]
[5M]
[5M]
[10M]
[10M]
[10M]

Prepared by: **B.VENKATESU**

ADVANCED DSP & APPLICATIONS



SIDDHARTH GROUP OF INSTITUTIONS :: PUTTUR

Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK (DESCRIPTIVE)

Subject with Code : ADSP&A(16EC5504)

Branch& Specialization: ECE-ES

Year & Sem: M.TECH-I SEM

<u>UNIT –IV</u>

ANANLYSIS OF FINITE WORLD LENGTH EFFECTS

1.(a) Explain the quantization by truncation and rounding method.	[5M]
(b)Explain zero input and overflow limit cycle oscillations with respect to finite word length	
effects.	[5M]
2. (a) Discuss about fast DFT algorithm based on index mapping.	[5M]
(b)Write a short note on narrow frequency band of DFT.	[5M]
3. (a) What are the errors that effect using feedback?	[5M]
(b)Write the limits of IIR digital filters.	[5M]
4. (a) Illustrate the process of quantization of fixed point and floating point numbers in the analy	ysis of
finite word length effects.	[5M]
(b)Explain the effect of input scaling on signal to noise ratio (SNR).	[5M]
5. (a)Consider a second order digital filter structure and find its model for product round-off error	or
analysis with an example.	[5M]
(b)Discuss about round-off errors in FFT algorithm.	[5M]
6. (a) Using an example, explain how the quantization of fixed point numbers is carried out.	[5M]
(b). Write short notes on analysis of coefficient quantization effects.	[5M]
7. (a) Discuss what do you mean by dynamic range scaling.	[5M]
(b).Explain how round of errors in FFT algorithms is done.	[5M]
8.(a) Write short notes on analysis of coefficient quantization effects in FIR filters.	[5M]
(b).Using a model diagram, explain A/D conversion noise analysis.	[5M]
9. (a)Discuss about quantization process and explain quantization of fixed-point numbers.	[5M]
(b).Write a short note on dynamic range scaling	[5M]
10. (a) What do you mean by dynamic range scaling? Explain in detail.	[5M]
(b). How is the product round off errors reduced?	[5M]
	TECH

Prepared by: **B.VENKATESU**

ADVANCED DSP & APPLICATIONS

QUESTION BANK	2016
---------------	------

SIDDHARTH GROUP OF INSTITUTIONS :: PUTTUR

Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK (DESCRIPTIVE)

Subject with Code : ADSP&A(16EC5504) Branch& Specialization: ECE-ES

Year & Sem: M.TECH-I SEM

<u>UNIT –V</u>

APPLICATIONS OF DSP & MULTIRATE SIHNAL PROCESSING

technical details.[5](b).Explain any two applications of DSP processors.[5]2. (a) What are the current trends in digital signal processors?[5]	M] M]
	M]
2. (a) What are the current trends in digital signal processors? [5N	_
	M]
(b).Write the applications of DSP processor. [5N	
3. Write the following:	
(a)Spectral analysis of non-stationary signals. [5M	M]
(b)Over sampling D/A converter. [5M	M]
4. (a) Give the functional diagram of DSP processor TMS320C50 and explain the importance of each	
block briefly. [5N	M]
(b).List out the addressing modes in a DSP processor. [5M	M]
5. (a) With DFT sample figures explain dual tone multi frequency signal detection. [5M	M]
(b)Discuss the effect of over sampling A/D converter [5M	M]
6. (a) Explain the process of spectral analysis of non-stationary signals. [5]	M]
(b)Discuss the effect of over sampling D/A convertor. [5M	M]
7. Write short notes on:	
(a).DSP controller. [5M	M]
(b).Musical sound processing [5M	M]
8. (a) Describe musical sound processing. [5M	M]
(b)Explain the following:	
(i) Oversampling A/D converter. (ii) Oversampling D/A converter. [5N	M]

QUESTION BANK	2016
9. (a) Explain the architecture of TMS 320C54 DSP.	[5M]
(b).Define multirate systems and sampling rate conversion	[5M]
10.(a). Explain the effects of over sampling for ADC and DAC.(b). With the help of block diagram explain the architecture of digital signal processors	[5M] [5M]

Prepared by: **B.VENKATESU**